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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Rajesh Khamankar, et al. Docket No: TI-33223
Serial No: 10/702,234 Conf. No: 7943
Examiner: Nathan W. Ha Art Unit: 2814
Filed: 11/06/2003
For: RELIABLE HIGH VOLTAGE GATE DIELECTRIC LAYERS USING A DUAL NITRIDATION
PROCESS

ELECTION

Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

MAILING CERTIFICATE UNDER 37 C.F.R. § 1.8(a)
I hereby certify that the above correspondence is being
deposited with the U.S. Postal Service with sufficient
postage as First Class Mail in an envelope addressed to:
Commissioner for Patents, P.O. Box 1450, Alexandria, VA
22313-1450 on 10-5-04.


Ann Trent

Dear Sir:

This election is offered in response to the Examiner's restriction requirement mailed
September 9, 2004.

Applicants hereby elect to pursue Group II of Claims 1-8, drawn to a method of
making a semiconductor device, without traversing the Examiner's restriction requirement.

Respectfully submitted,


Peter K. McLarty
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